

Raul Camposano

rcw@camposano.com

Professional activities

Societies

- IEEE Fellow, ACM, IFIP WG 10.5
 - IEC Executive Council, since 2000
 - Chair of IFIP TC 10 WG 10.2, 1992-1995
-

Journals Editorships

- Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1991 to present
 - Editor of Foundations and Trends in EDA, 2006 to present
 - Editor of Integration, the VLSI journal, 1991 to present
 - Editor in Chief of Design Automation for Embedded Systems, 1995 – 2005
 - Advisory Board of Design Automation for Embedded Systems, 2005 – present
 - Editorial Board of Foundations and Trends in Electronic Design Automation, 2005-present
 - Regional Editor for Europe, VLSI Design, 1992 to 1995
 - Editorial board of the Journal of Microelectronics System Integration, 1992 to 1995
 - Associate Editor, International Journal of Computer Aided VLSI Design, 1991
-

Conference Committees

- DAC technical program committee, 1996 - 1997
 - ICCAD Executive committee member, European representative, TPC, 1990 - 1993
 - ICCD General Chair, TPC Chair, TPC, 1988 - 1993
 - EURO-DAC General Chair, Vice-Chair and tutorial chair, 1992 - 1993
 - ISSS technical program committee 1997 – 2002
 - CODES+ISSS technical program committee 2003-2005
 - SBCCI technical program committee, 2001, 2002
 - VLSI technical program committee, 1989
 - CHDL technical program committee, 1991 - 1999
 - EDAC technical program committee, 1990 - 1993
 - EURO-VHDL technical program committee, 1992 - 1993
 - Asia-Pacific Conference on Hardware Description, TPC Chair, TPC 1993 – 1997
-

Workshops Committees

- First ACM conference on Languages Compilers and Tools for Embedded Systems, TPC 2002
- International Workshop on Hardware/Software Co-design (CODES), TPC 1999-2002
- ACM/IEEE Int. WS on High-Level Synthesis: TPC, TPC Chair and General Chair 1988-1991
- Physical Design Workshop on Module Generation and Silicon Compilation: TPC 1989
- IEEE VHDL Methods Workshop: TPC 1989
- Second European Conference on VHDL Methods: TPC 1991
- TAU: TPC 1992 and general chair 1993
- International Workshop on HW/SW Co-design: TPC 1992-1999
- EURO ASIC: TPC 1992
- WS on Synthesis Generation and Portability of Library Blocks for ASIC Design: TPC 1992
- IFIP WS on Control Dominated Synthesis from a RTL Description: TPC 1992
- ITG/GI/GME Rechnergestuetzter Entwurf und Architektur mikroelektronischer Systeme 1992

University courses, seminars, tutorials

University of Karlsruhe, Germany

- Design Automation for VLSI
 - Seminars: Petri-Nets,
 - The impact of VLSI on digital circuit design
-

University of Siegen, Germany

- Introduction to integrated circuit design
 - Automata theory and formal languages
-

Universidad del Norte, Chile

- Automata theory and formal languages
 - Operating systems
-

University of Paderborn, Germany

- High-Level synthesis
 - Synthesis of digital circuits I + II
-

Tutorials and Short Courses

- EDA, Semiconductor IC Design&Applications, Stanford Engineering and Science Institute, August 2004
- Spring 99 seminar series on "System-on-Chip Design", Stanford University, April 1999
- System Level PATO class: Modeling and Synthesis of Behavior, Control, and Dataflow, Delft, The Netherlands, June 1998
- Modeling and Synthesis of Behavior, Control, and Dataflow ICCAD, San Jose, CA, 1997
- High-Level Design, Lipari, Italy, 1997
- Behavioral Synthesis, DAC, Las Vegas, 1996
- Performance Driven Behavioral Synthesis, ASP-DAC, CHDL, VLSI, Tokyo, 1995
- A Review of Hardware Synthesis Techniques: Behavioral Synthesis, NATO Advanced Study Institute on HW/SW Co-design, Tremezzo, Italy, 1995
- EUROCHIP advanced course on High-Level Digital System Design, 1994, "High-Level Synthesis"
- Behavioral Synthesis: From Research to Production Use, ICCAD, Santa Clara, 1994
- EUROCHIP advanced course on High-Level Digital System Design, 1993, "Generic Design Techniques: Introduction" and "High-Level Design"
- System Level Synthesis, ASP CHDL, Brisbane, Australia, 1993
- High-Level Synthesis, GRIAO, Montreal, 1992
- EUROCHIP advanced course on High-Level Digital System Design, 1992, "Computational Structures and Design Automation" and "High-Level Design"
- High-Level Synthesis, EDAC'92
- High-level Design, Porto Alegre, Brasil, 1991
- High-Level Synthesis of Digital Circuits: HDL to Logic, DAC'91
- Tutorial on High-Level Synthesis, ICCAD'90
- High-Level Synthesis, EDAC'90
- Scheduling and Allocation Algorithms for HLS, IBM Lectures in Computer Science, 1989-1990
- Hardware Description Languages for Synthesis, DAC'89
- High-Level Synthesis, ISCAS'89
- Tools for Digital Systems Design, University of Chile, Santiago, Chile, 1987
- Structural Synthesis (Advanced Study Institute on Logic Synthesis and Silicon Compilation for VLSI Design, L'Aquila, Italy, July 13-18, 1987)